DAN28027

Two 12 bit ADC Inputs and Two 20KHz Carrier Frequency PWM Outputs with SPI Interface

Features:

- Operating Voltage 3.3Volts.
- Two 12 bit SAR ADCs with 0V to 3.3V range.
- Two PWM Outputs, 20KHz Carrier Frequency for driving H-bridge DC Motor amplifiers through the DIR (Direction) Input.
- SPI Interface, Standard 4-wire connection MOSI, MISO, SS\, SCLK, Slave Mode Only.
- SPI maximum SCLK rate of 1 MHz.

General Description

The DAN28027 is an integrated circuit chip (IC) that adds two 12 bit ADC inputs and two PWM outputs for driving DC motors in your embedded system. It uses standard 4-wire SPI serial communication and the DAN28027 is a SPI slave only device.

The two ADC channels are SAR (Successive Approximation Register) type ADCs with an input range of 0 to 3.3Volts. With 12 bits, that gives an input resolution of 3.3Volts/4095.0 steps. The DAN28027 continuously samples the two ADC channels every 1 millisecond and the most current samples are transmitted to the SPI Master when the SPI Master issues a read/write command.

The two PWM outputs are driven with a 20Khz carrier frequency. These two PWM's could then each drive an H-bridge device. This PWM should drive the direction (DIR) pin of the H-bridge. For example, the A4973 H-bridge works well having its DIR pin driven with a PWM signal. 0% duty cycle drives the DC motor in the negative direction with full torque. 50% duty cycle is zero torque to the DC motor. 100% duty cycle drives the DC motor in the positive direction with full torque. So for example 75% duty cycle drives the DC motor in the positive direction with 50% of the full torque. Each PWM channel has a resolution of 3000 steps where 0 is 0% duty cycle, 1500 is 50% duty cycle and 3000 is 100% duty cycle.

Device Pins

Vcc: 3.3V power for the IC

Gnd: Ground of the 3.3V power

ADC1: ADC channel one's input pin. Accepts a voltage in the range of 0 to 3.3 volts. Value communicated over SPI is an integer with the range of 0 to 4095 where 0 equals 0 volts and 4095 equals 3.3volts.

ADC2: ADC channel two's input pin. Accepts a voltage in the range of 0 to 3.3 volts. Value communicated over SPI is an integer with the range of 0 to 4095 where 0 equals 0 volts and 4095 equals 3.3volts.

PWM1: H-bridge/DC motor command output one. 20KHz Carrier Frequency. 0% to 100% duty cycle command where 0% duty cycle is commanded with the value 0, 50% duty cycle is commanded with the value 1500, and 100% duty cycle is commanded with the value 3000. So CommandtoSend = percent_duty_cycle * 3000.0/100.0.

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PWM2: H-bridge/DC motor command output one. 20KHz Carrier Frequency. 0% to 100% duty cycle command where 0% duty cycle is commanded with the value 0, 50% duty cycle is commanded with the value 1500, and 100% duty cycle is commanded with the value 3000. So CommandtoSend = percent_duty_cycle * 3000.0/100.0.

SPI_SS: Slave Select, Active Low. Slave select must be held for the entire SPI communication to the DAN28027. If high the DAN28027 is not selected and no communication can occur.

SPI_SCLK: SPI CLK Clock is normally low when no communication is in progress. During communication, both the SPI master and SPI slave read in a new bit on the rising edge of the SCLK. The SPI master reads the new bit (1 or 0) of the MISO pin. The SPI slave reads the new bit (1 or 0) of the MOSI pin.

SPI_MOSI: SPI Slave Input pin. PWM commands are received on this pin from the master.

SPI_MISO: SPI Slave Output pin. ADC result values are transmitted on this pin to the master.

LED: DAN28027 running status. When wired to an LED, this pin that indicates if the DAN28027 chip is operating. When powered, the DAN28027 chip will blink on and off the connected LED.

Reset: This pin should be wired to a pushbutton. Used to reset the program running on the DAN28027 back to the beginning of its code. This is a nice feature when debugging the SPI Master's code. Whenever the SPI Master code is restarted, the DAN28027 should be reset by pressing this button, in order that the SPI communication is in sync.

RESERVED: Reserved for future use in new releases of the DAN28027.

Registers in the DAN28027 chip accessible through the SPI interface.

ADC1: Value between 0 and 4095

ADC1: (Register size: 16 bits, value 12 bits, only uses bottom 12 bits of register. Upper 4 bits always zero.)

ADC1 voltage reading received over SPI. This returned value, has a range from 0 to 4095 where 0 is 0V and 4095 is 3.3V

ADC2: Value between 0 and 4095

ADC2: (Register size: 16 bits, value 12 bits, only uses bottom 12 bits of register. Upper 4 bits always zero.)

ADC2 voltage reading received over SPI. This returned value, has a range from 0 to 4095 where 0 is 0V and 4095 is 3.3V

PWM1: Value between 0 and 3000

PWM1: (Register size 16bits, value 12 bits, only uses bottom 12 bits of register. Upper 4 bits should always be zero)

20KHz carrier frequency PWM signa1, 0 = 0% duty cycle, 1500 = 50% duty cycle and 3000 = 100% duty cycle.

If the DAN28027 receives a value greater than 3000, the value of 3000 or 100% duty cycle is applied.
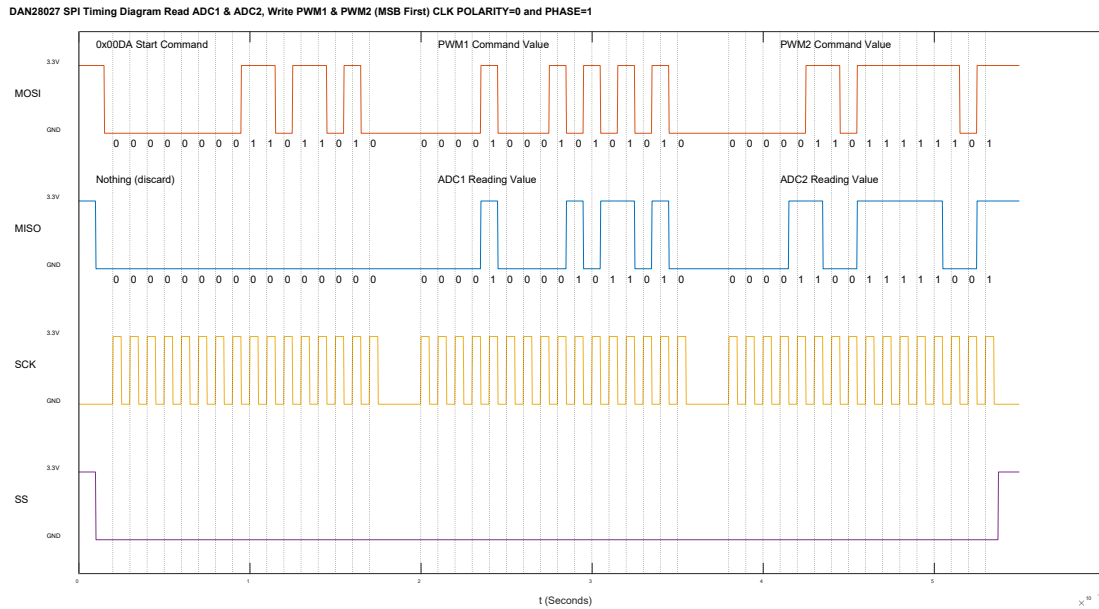
PWM2: Value between 0 and 3000

PWM2: (Register size 16bits, value 12 bits, only uses bottom 12 bits of register. Upper 4 bits should always be zero)

20KHz carrier frequency PWM signa1, 0 = 0% duty cycle, 1500 = 50% duty cycle and 3000 = 100% duty cycle.

If the DAN28027 receives a value greater than 3000, the value of 3000 or 100% duty cycle is applied.

SPI Interface

DAN28027 SPI Timing Diagram Read ADC1 & ADC2, Write PWM1 & PWM2 (MSB First) CLK POLARITY=0 and PHASE=1

Each time the SPI master needs to communicate with the DAN28027 the above timing diagram must be followed:

1. SS\ must be pulled low by the SPI Master.
2. 0x00DA must be sent as the first 16 bit value. During this transmission of 0x00DA, the DAN28027 sends nothing important back to the Master so this 16 bit value can be discarded once read on the Master's end.
3. SPI master sends the 16 bit PWM1 command value between 0 and 3000. During this transmission, ADC1's 16 bit value is sent to the SPI Master.
4. SPI master sends the 16 bit PWM2 command value between 0 and 3000. During this transmission, ADC2's 16 bit value is sent to the SPI Master.
5. SS\ must be pulled high by the SPI Master.