Low Cost Low Power Instrumentation Amplifier

AD620

FEATURES

Easy to use
- Gain set with one external resistor
  - (Gain range 1 to 10,000)
- Wide power supply range (±2.3 V to ±18 V)
- Higher performance than 3 op amp IA designs
- Available in 8-lead DIP and SOIC packaging
- Low power, 1.3 mA max supply current

Excellent dc performance (B grade)
- 50 µV max, input offset voltage
- 0.6 µV/°C max, input offset drift
- 1.0 nA max, input bias current
- 100 dB min common-mode rejection ratio (G = 10)

Low noise
- 9 nV/√Hz @ 1 kHz, input voltage noise
- 0.28 µV p-p noise (0.1 Hz to 10 Hz)

Excellent ac specifications
- 120 kHz bandwidth (G = 100)
- 15 µs settling time to 0.01%

APPLICATIONS

Weigh scales
ECG and medical instrumentation
Transducer interface
Data acquisition systems
Industrial process controls
Battery-powered and portable equipment

CONNECTION DIAGRAM

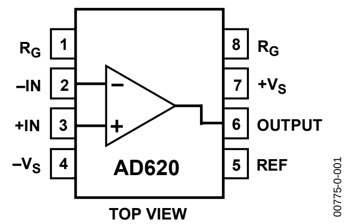

Figure 1. 8-Lead PDIP (N), CERDIP (Q), and SOIC (R) Packages

PRODUCT DESCRIPTION

The AD620 is a low cost, high accuracy instrumentation amplifier that requires only one external resistor to set gains of 1 to 10,000. Furthermore, the AD620 features 8-lead SOIC and DIP packaging that is smaller than discrete designs and offers lower power (only 1.3 mA max supply current), making it a good fit for battery-powered, portable (or remote) applications.

The AD620, with its high accuracy of 40 ppm maximum nonlinearity, low offset voltage of 50 µV max, and offset drift of 0.6 µV/°C max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias current, and low power of the AD620 make it well suited for medical applications, such as ECG and noninvasive blood pressure monitors.

The low input bias current of 1.0 nA max is made possible with the use of Superϐeta processing in the input stage. The AD620 works well as a preamplifier due to its low input voltage noise of 9 nV/√Hz at 1 kHz, 0.28 µV p-p in the 0.1 Hz to 10 Hz band, and 0.1 pA/√Hz input current noise. Also, the AD620 is well suited for multiplexed applications with its settling time of 15 µs to 0.01%, and its cost is low enough to enable designs with one in-amp per channel.

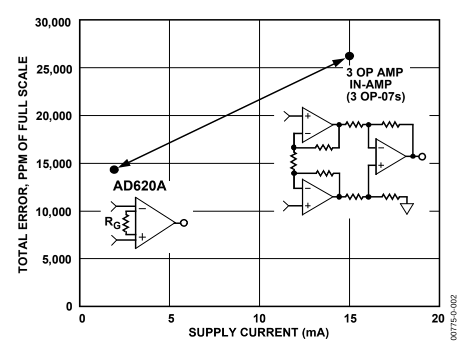

Figure 2. Three Op Amp IA Designs vs. AD620

Table 1. Next Generation Upgrades for AD620

Part	Comment
AD8221	Better specs at lower price
AD8222	Dual channel or differential out
AD8226	Low power, wide input range
AD8220	JFET input
AD8228	Best gain accuracy
AD8295	+2 precision op amps or differential out
AD8429	Ultra low noise

Rev. H

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SPECIFICATIONS

Typical @ 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

Table 2.

Parameter	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Unit
GAIN	G = 1 + (49.4 kΩ/R_G)										
Gain Range		1		10,000	1		10,000	1		10,000	
Gain Error[2]	V_{OUT} = ±10 V										
G = 1			0.03	0.10		0.01	0.02		0.03	0.10	%
G = 10			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 100			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 1000			0.40	0.70		0.35	0.50		0.40	0.70	%
Nonlinearity	V_{OUT} = −10 V to +10 V										
G = 1–1000	R_L = 10 kΩ		10	40		10	40		10	40	ppm
G = 1–100	R_L = 2 kΩ		10	95		10	95		10	95	ppm
Gain vs. Temperature											
	G = 1			10			10			10	ppm/°C
	Gain >1[2]			−50			−50			−50	ppm/°C
VOLTAGE OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)										
Input Offset, V_{OSI}	V_S = ±5 V to ± 15 V		30	125		15	50		30	125	µV
Overtemperature	V_S = ±5 V to ± 15 V			185			85			225	µV
Average TC	V_S = ±5 V to ± 15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
Output Offset, V_{OSO}	V_S = ±15 V		400	1000		200	500		400	1000	µV
	V_S = ± 5 V			1500			750			1500	µV
Overtemperature	V_S = ±5 V to ± 15 V			2000			1000			2000	µV
Average TC	V_S = ±5 V to ± 15 V		5.0	15		2.5	7.0		5.0	15	µV/°C
Offset Referred to the Input vs. Supply (PSR)	V_S = ±2.3 V to ±18 V										
G = 1		80	100		80	100		80	100		dB
G = 10		95	120		100	120		95	120		dB
G = 100		110	140		120	140		110	140		dB
G = 1000		110	140		120	140		110	140		dB
INPUT CURRENT											
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
Overtemperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
Overtemperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10‖2			10‖2			10‖2		GΩ_pF
Common-Mode			10‖2			10‖2			10‖2		GΩ_pF
Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$-V_S + 1.9$		$+V_S - 1.2$	$-V_S + 1.9$		$+V_S - 1.2$	$-V_S + 1.9$		$+V_S - 1.2$	V
Overtemperature		$-V_S + 2.1$		$+V_S - 1.3$	$-V_S + 2.1$		$+V_S - 1.3$	$-V_S + 2.1$		$+V_S - 1.3$	V
	V_S = ± 5 V to ±18 V	$-V_S + 1.9$		$+V_S - 1.4$	$-V_S + 1.9$		$+V_S - 1.4$	$-V_S + 1.9$		$+V_S - 1.4$	V
Overtemperature		$-V_S + 2.1$		$+V_S - 1.4$	$-V_S + 2.1$		$+V_S + 2.1$	$-V_S + 2.3$		$+V_S - 1.4$	V

Parameter	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Unit
Common-Mode Rejection											
Ratio DC to 60 Hz with											
1 kΩ Source Imbalance	V_{CM} = 0 V to ± 10 V										
G = 1		73	90		80	90		73	90		dB
G = 10		93	110		100	110		93	110		dB
G = 100		110	130		120	130		110	130		dB
G = 1000		110	130		120	130		110	130		dB
OUTPUT											
Output Swing	R_L = 10 kΩ										
	V_S = ±2.3 V to ± 5 V	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	V
Overtemperature		$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.6		$+V_S$ − 1.3	V
	V_S = ±5 V to ± 18 V	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	V
Overtemperature		$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 2.3		$+V_S$ − 1.5	V
Short Circuit Current			±18			±18			±18		mA
DYNAMIC RESPONSE											
Small Signal −3 dB Bandwidth											
G = 1			1000			1000			1000		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			12			12			12		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/μs
Settling Time to 0.01%	10 V Step										
G = 1–100			15			15			15		μs
G = 1000			150			150			150		μs
NOISE											
Voltage Noise, 1 kHz	$Total\ RTI\ Noise = \sqrt{(e^2_{ni}) + (e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			9	13		9	13		9	13	nV/√Hz
Output, Voltage Noise, e_{no}			72	100		72	100		72	100	nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0	6.0		3.0	6.0	μV p-p
G = 10			0.55			0.55	0.8		0.55	0.8	μV p-p
G = 100–1000			0.28			0.28	0.4		0.28	0.4	μV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
0.1 Hz to 10 Hz			10			10			10		pA p-p
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		50	60		50	60		50	60	μA
Voltage Range		$-V_S$ + 1.6		$+V_S$ − 1.6	$-V_S$ + 1.6		$+V_S$ − 1.6	$-V_S$ + 1.6		$+V_S$ − 1.6	V
Gain to Output		1 ± 0.0001			1 ± 0.0001			1 ± 0.0001			
POWER SUPPLY											
Operating Range[4]		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
Overtemperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance		−40 to +85			−40 to +85			−55 to +125			°C

[1] See Analog Devices military data sheet for 883B tested specifications.
[2] Does not include effects of external resistor R_G.
[3] One input grounded. G = 1.
[4] This is defined as the same supply range that is used to specify PSR.

THEORY OF OPERATION

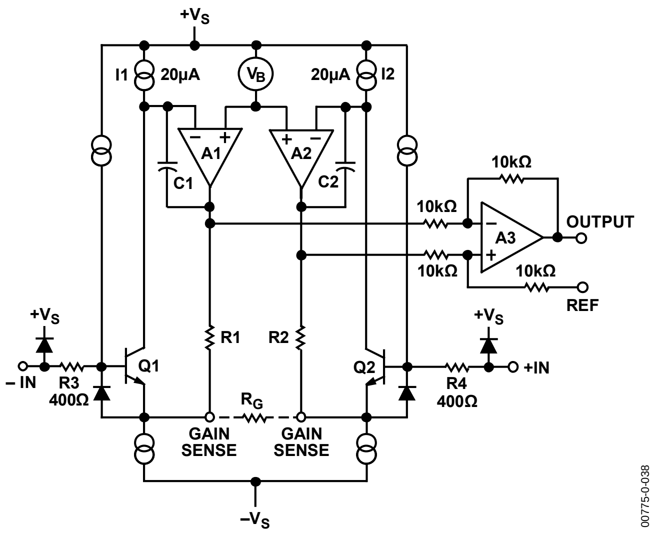

Figure 36. Simplified Schematic of AD620

The AD620 is a monolithic instrumentation amplifier based on a modification of the classic three op amp approach. Absolute value trimming allows the user to program gain *accurately* (to 0.15% at G = 100) with only one resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components, thus ensuring the high level of performance inherent in this circuit.

The input transistors Q1 and Q2 provide a single differential-pair bipolar input for high precision (Figure 36), yet offer 10× lower input bias current thanks to Superβeta processing. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains constant collector current of the input devices Q1 and Q2, thereby impressing the input voltage across the external gain setting resistor R_G. This creates a differential gain from the inputs to the A1/A2 outputs given by $G = (R1 + R2)/R_G + 1$. The unity-gain subtractor, A3, removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: (a) Open-loop gain is boosted for increasing programmed gain, thus reducing gain related errors. (b) The gain-bandwidth product (determined by C1 and C2 and the preamp transconductance) increases with programmed gain, thus optimizing frequency response. (c) The input voltage noise is reduced to a value of 9 nV/√Hz, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor.

The gain equation is then

$$G = \frac{49.4k\Omega}{R_G} + 1$$

$$R_G = \frac{49.4k\Omega}{G-1}$$

Make vs. Buy: a Typical Bridge Application Error Budget

The AD620 offers improved performance over "homebrew" three op amp IA designs, along with smaller size, fewer components, and 10× lower supply current. In the typical application, shown in Figure 37, a gain of 100 is required to amplify a bridge output of 20 mV full-scale over the industrial temperature range of −40°C to +85°C. Table 4 shows how to calculate the effect various error sources have on circuit accuracy.

Regardless of the system in which it is being used, the AD620 provides greater accuracy at low power and price. In simple systems, absolute accuracy and drift errors are by far the most significant contributors to error. In more complex systems with an intelligent processor, an autogain/autozero cycle removes all absolute accuracy and drift errors, leaving only the resolution errors of gain, nonlinearity, and noise, thus allowing full 14-bit accuracy.

Note that for the homebrew circuit, the OP07 specifications for input voltage offset and noise have been multiplied by √2. This is because a three op amp type in-amp has two op amps at its inputs, both contributing to the overall input error.

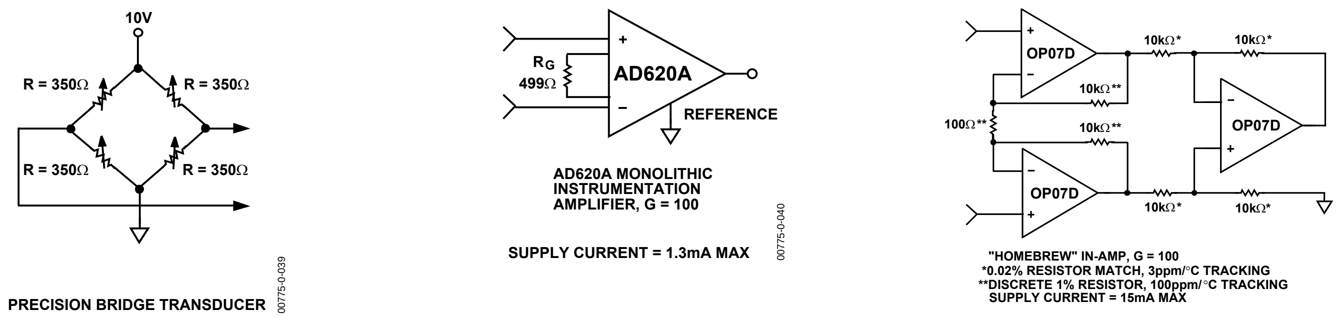

Figure 37. Make vs. Buy

Table 4. Make vs. Buy Error Budget

Error Source	AD620 Circuit Calculation	"Homebrew" Circuit Calculation	Error, ppm of Full Scale AD620	Homebrew
ABSOLUTE ACCURACY at T_A = 25°C				
Input Offset Voltage, µV	125 µV/20 mV	(150 µV × √2)/20 mV	6,250	10,607
Output Offset Voltage, µV	1000 µV/100 mV/20 mV	((150 µV × 2)/100)/20 mV	500	150
Input Offset Current, nA	2 nA ×350 Ω/20 mV	(6 nA ×350 Ω)/20 mV	18	53
CMR, dB	110 dB(3.16 ppm) ×5 V/20 mV	(0.02% Match × 5 V)/20 mV/100	791	500
		Total Absolute Error	7,559	11,310
DRIFT TO 85°C				
Gain Drift, ppm/°C	(50 ppm + 10 ppm) ×60°C	100 ppm/°C Track × 60°C	3,600	6,000
Input Offset Voltage Drift, µV/°C	1 µV/°C × 60°C/20 mV	(2.5 µV/°C × √2 × 60°C)/20 mV	3,000	10,607
Output Offset Voltage Drift, µV/°C	15 µV/°C × 60°C/100 mV/20 mV	(2.5 µV/°C × 2 × 60°C)/100 mV/20 mV	450	150
		Total Drift Error	7,050	16,757
RESOLUTION				
Gain Nonlinearity, ppm of Full Scale	40 ppm	40 ppm	40	40
Typ 0.1 Hz to 10 Hz Voltage Noise, µV p-p	0.28 µV p-p/20 mV	(0.38 µV p-p × √2)/20 mV	14	27
		Total Resolution Error	54	67
		Grand Total Error	14,663	28,134

G = 100, V_S = ±15 V.
(All errors are min/max and referred to input.)

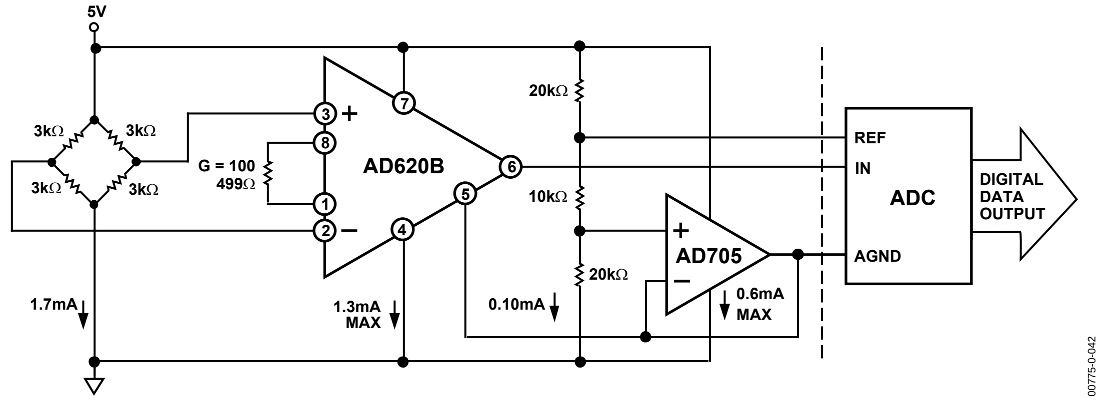

Figure 38. A Pressure Monitor Circuit that Operates on a 5 V Single Supply

Pressure Measurement

Although useful in many bridge applications, such as weigh scales, the AD620 is especially suitable for higher resistance pressure sensors powered at lower voltages where small size and low power become more significant.

Figure 38 shows a 3 kΩ pressure transducer bridge powered from 5 V. In such a circuit, the bridge consumes only 1.7 mA. Adding the AD620 and a buffered voltage divider allows the signal to be conditioned for only 3.8 mA of total supply current.

Small size and low cost make the AD620 especially attractive for voltage output pressure transducers. Since it delivers low noise and drift, it also serves applications such as diagnostic noninvasive blood pressure measurement.

Medical ECG

The low current noise of the AD620 allows its use in ECG monitors (Figure 39) where high source resistances of 1 MΩ or higher are not uncommon. The AD620's low power, low supply voltage requirements, and space-saving 8-lead mini-DIP and SOIC package offerings make it an excellent choice for battery-powered data recorders.

Furthermore, the low bias currents and low current noise, coupled with the low voltage noise of the AD620, improve the dynamic range for better performance.

The value of capacitor C1 is chosen to maintain stability of the right leg drive loop. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

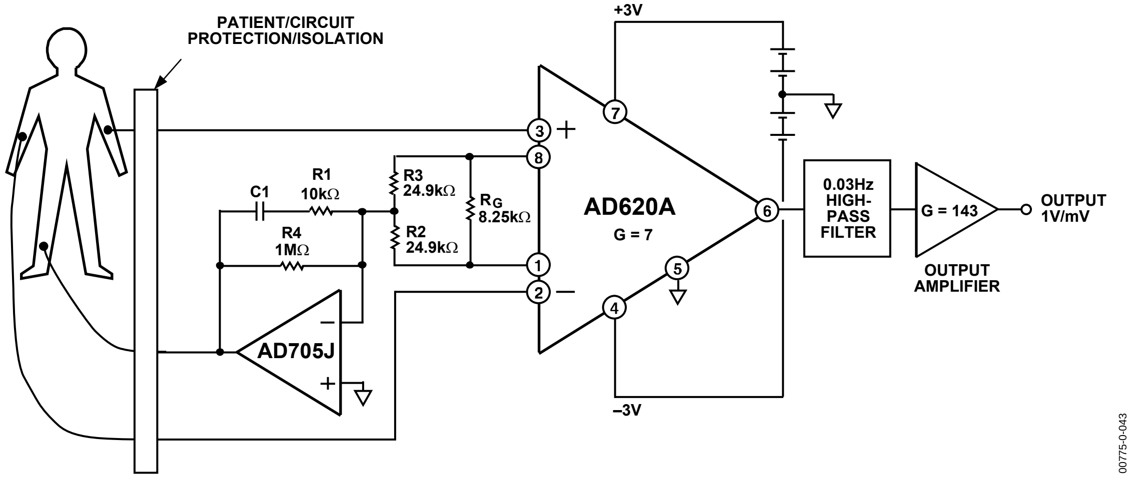

Figure 39. A Medical ECG Monitor Circuit

Precision V-I Converter

The AD620, along with another op amp and two resistors, makes a precision current source (Figure 40). The op amp buffers the reference terminal to maintain good CMR. The output voltage, V_X, of the AD620 appears across R1, which converts it to a current. This current, less only the input bias current of the op amp, then flows out to the load.

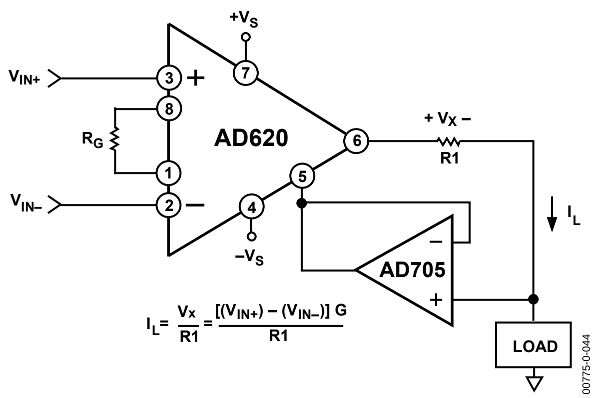

Figure 40. Precision Voltage-to-Current Converter (Operates on 1.8 mA, ±3 V)

GAIN SELECTION

The AD620 gain is resistor-programmed by R_G, or more precisely, by whatever impedance appears between Pins 1 and 8. The AD620 is designed to offer accurate gains using 0.1% to 1% resistors. Table 5 shows required values of R_G for various gains. Note that for G = 1, the R_G pins are unconnected ($R_G = \infty$). For any arbitrary gain, R_G can be calculated by using the formula:

$$R_G = \frac{49.4\,k\Omega}{G-1}$$

To minimize gain error, avoid high parasitic resistance in series with R_G; to minimize gain drift, R_G should have a low TC—less than 10 ppm/°C—for the best performance.

Table 5. Required Values of Gain Resistors

1% Std Table Value of R_G(Ω)	Calculated Gain	0.1% Std Table Value of R_G(Ω)	Calculated Gain
49.9 k	1.990	49.3 k	2.002
12.4 k	4.984	12.4 k	4.984
5.49 k	9.998	5.49 k	9.998
2.61 k	19.93	2.61 k	19.93
1.00 k	50.40	1.01 k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003.0

INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD620 are attributed to two sources, input and output errors. The output error is divided by *G* when referred to the input. In practice, the input errors dominate at high gains, and the output errors dominate at low gains. The total V_{OS} for a given gain is calculated as

Total Error RTI = input error + (output error/G)

Total Error RTO = (input error × G) + output error

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

INPUT PROTECTION

The AD620 safely withstands an input current of ±60 mA for several hours at room temperature. This is true for all gains and power on and off, which is useful if the signal source and amplifier are powered separately. For longer time periods, the input current should not exceed 6 mA.

For input voltages beyond the supplies, a protection resistor should be placed in series with each input to limit the current to 6 mA. These can be the same resistors as those used in the RFI filter. High values of resistance can impact the noise and AC CMRR performance of the system. Low leakage diodes (such as the BAV199) can be placed at the inputs to reduce the required protection resistance.

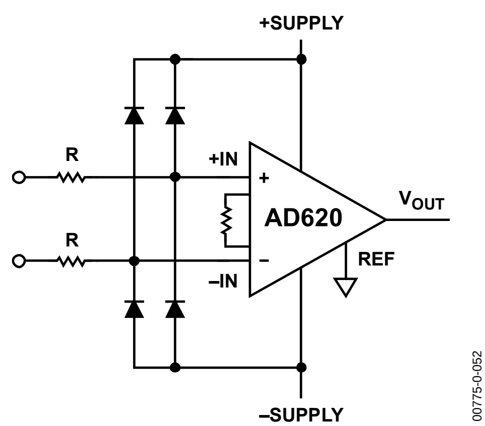

Figure 41. Diode Protection for Voltages Beyond Supply

RF INTERFERENCE

All instrumentation amplifiers rectify small out of band signals. The disturbance may appear as a small dc voltage offset. High frequency signals can be filtered with a low pass R-C network placed at the input of the instrumentation amplifier. Figure 42 demonstrates such a configuration. The filter limits the input signal according to the following relationship:

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$.

C_D affects the difference signal. C_C affects the common-mode signal. Any mismatch in $R \times C_C$ degrades the AD620 CMRR. To avoid inadvertently reducing CMRR-bandwidth performance, make sure that C_C is at least one magnitude smaller than C_D. The effect of mismatched C_Cs is reduced with a larger C_D:C_C ratio.

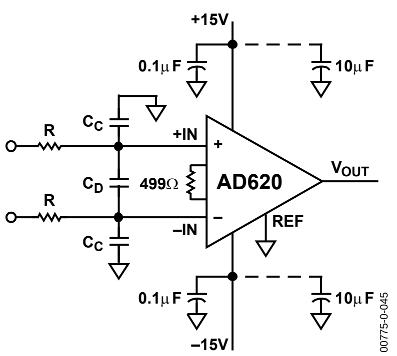

Figure 42. Circuit to Attenuate RF Interference

COMMON-MODE REJECTION

Instrumentation amplifiers, such as the AD620, offer high CMR, which is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

For optimal CMR, the reference terminal should be tied to a low impedance point, and differences in capacitance and resistance should be kept to a minimum between the two inputs. In many applications, shielded cables are used to minimize noise; for best CMR over frequency, the shield should be properly driven. Figure 43 and Figure 44 show active data guards that are configured to improve ac common-mode rejections by "bootstrapping" the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

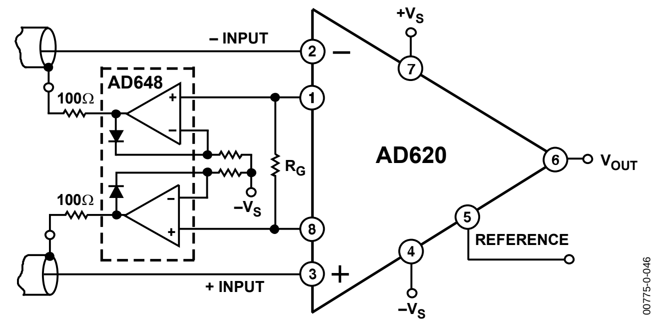

Figure 43. Differential Shield Driver

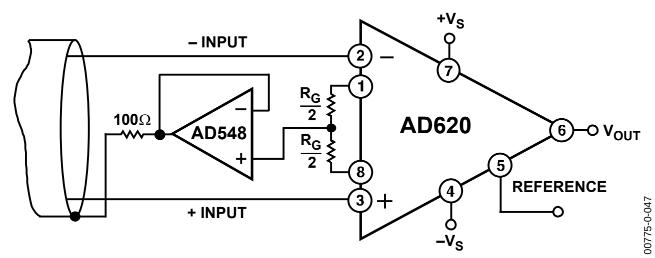

Figure 44. Common-Mode Shield Driver

GROUNDING

Since the AD620 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems by simply tying the REF pin to the appropriate "local ground."

To isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground pins (Figure 45). It would be convenient to use a single ground line; however, current through ground wires and PC runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground. These ground returns must be tied together at some point, usually best at the ADC package shown in Figure 45.

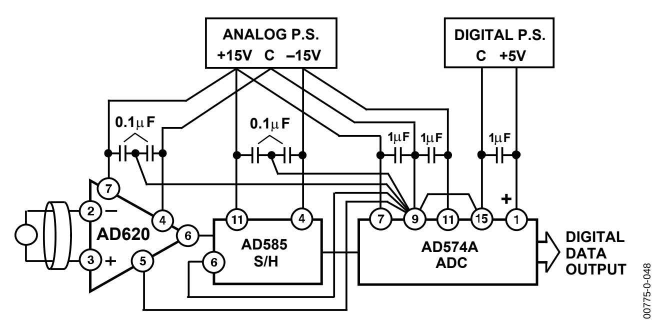

Figure 45. Basic Grounding Practice

GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of an amplifier. There must be a direct return path for these currents. Therefore, when amplifying "floating" input sources, such as transformers or ac-coupled sources, there must be a dc path from each input to ground, as shown in Figure 46, Figure 47, and Figure 48. Refer to *A Designer's Guide to Instrumentation Amplifiers* (free from Analog Devices) for more information regarding in-amp applications.

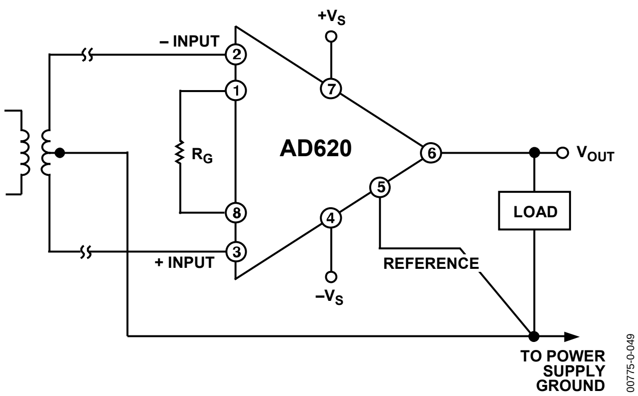

Figure 46. Ground Returns for Bias Currents with Transformer-Coupled Inputs

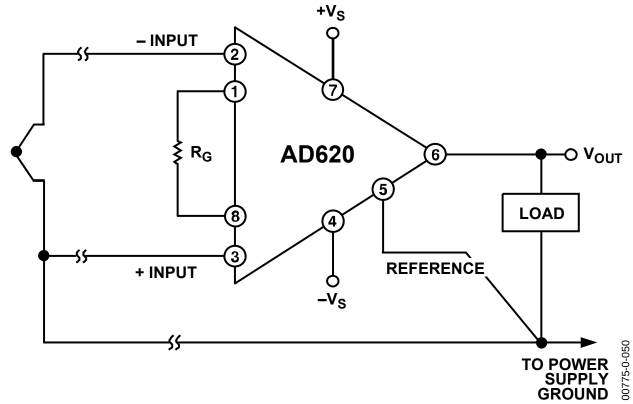

Figure 47. Ground Returns for Bias Currents with Thermocouple Inputs

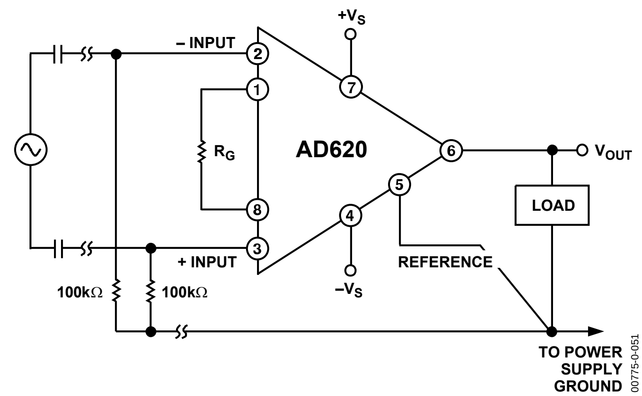

Figure 48. Ground Returns for Bias Currents with AC-Coupled Inputs

AD620ACHIPS INFORMATION

Die size: 1803 μm × 3175 μm

Die thickness: 483 μm

Bond Pad Metal: 1% Copper Doped Aluminum

To minimize gain errors introduced by the bond wires, use Kelvin connections between the chip and the gain resistor, R_G, by connecting Pad 1A and Pad 1B in parallel to one end of R_G and Pad 8A and Pad 8B in parallel to the other end of R_G. For unity gain applications where R_G is not required, Pad 1A and Pad 1B must be bonded together as well as the Pad 8A and Pad 8B.

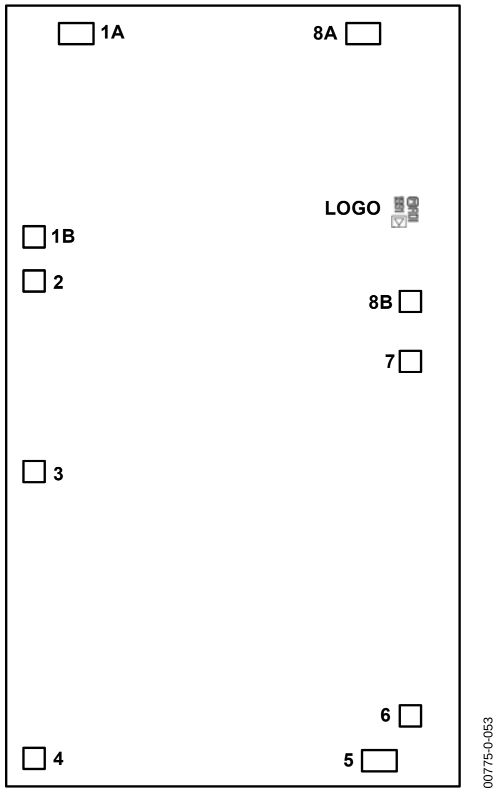

Figure 49. Bond Pad Diagram

Table 6. Bond Pad Information

Pad No.	Mnemonic	Pad Coordinates[1] X (μm)	Pad Coordinates[1] Y (μm)
1A	R_G	−623	+1424
1B	R_G	−789	+628
2	−IN	−790	+453
3	+IN	−790	−294
4	$-V_S$	−788	−1419
5	REF	+570	−1429
6	OUTPUT	+693	−1254
7	$+V_S$	+693	+139
8A	R_G	+505	+1423
8B	R_G	+693	+372

[1] The pad coordinates indicate the center of each pad, referenced to the center of the die. The die orientation is indicated by the logo, as shown in Figure 49.

OUTLINE DIMENSIONS

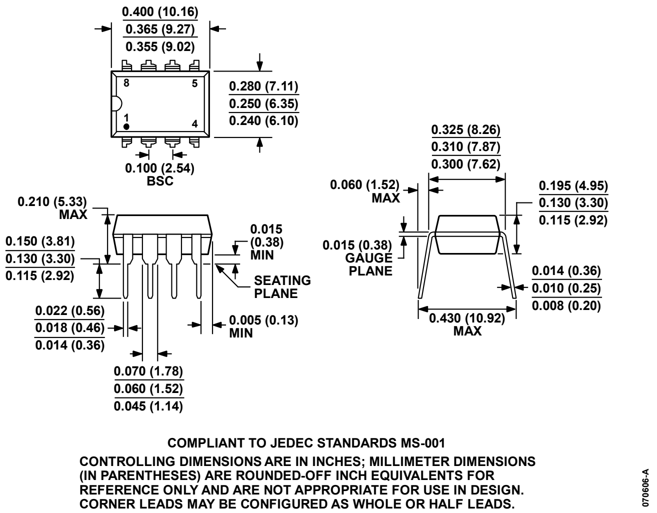

Figure 50. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body (N-8).
Dimensions shown in inches and (millimeters)

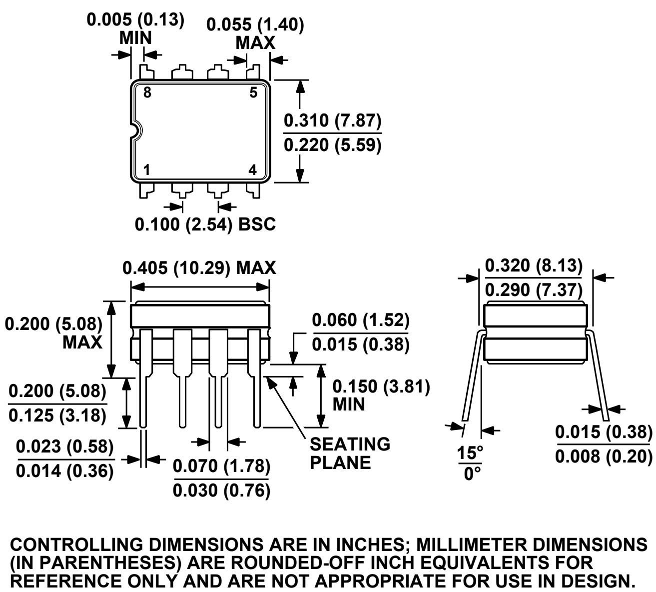

Figure 51. 8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)
Dimensions shown in inches and (millimeters)

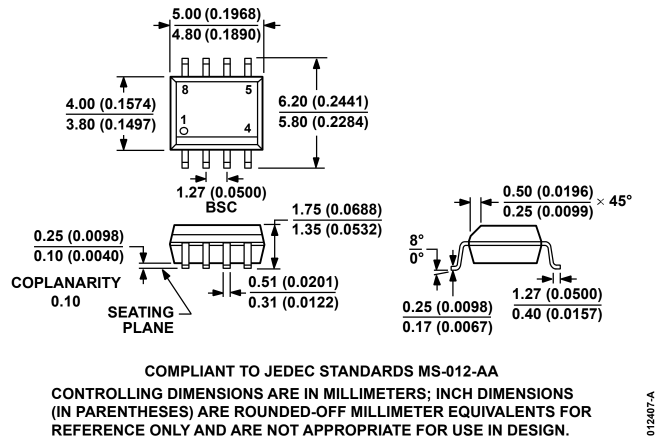

Figure 52. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD620AN	−40°C to +85°C	8-Lead PDIP	N-8
AD620ANZ	−40°C to +85°C	8-Lead PDIP	N-8
AD620BN	−40°C to +85°C	8-Lead PDIP	N-8
AD620BNZ	−40°C to +85°C	8-Lead PDIP	N-8
AD620AR	−40°C to +85°C	8-Lead SOIC_N	R-8
AD620ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD620AR-REEL	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD620ARZ-REEL	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD620AR-REEL7	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD620ARZ-REEL7	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD620BR	−40°C to +85°C	8-Lead SOIC_N	R-8
AD620BRZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD620BR-REEL	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD620BRZ-RL	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD620BR-REEL7	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD620BRZ-R7	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD620ACHIPS	−40°C to +85°C	Die Form	
AD620SQ/883B	−55°C to +125°C	8-Lead CERDIP	Q-8

[1] Z = RoHS Compliant Part.

C00775–0–7/11(H)